The NA62 Gigatracker: detector properties and pixel read-out architectures

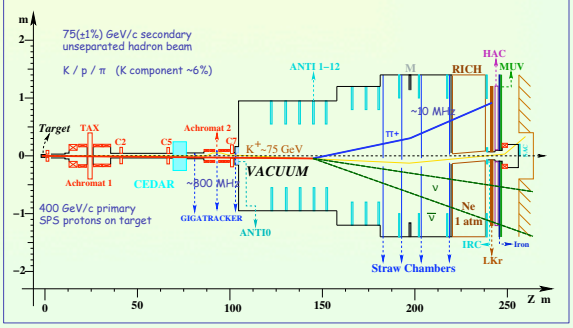
M. Fiorini[a], V. Carassiti[c], A. Ceccucci[a], E. Cortina[d], A. Cotta Ramusino[c], G. Dellacasa[b], P. Jarron[a], J. Kaplon[a], A. Kluge[a], F. Marchetto[b], E. Martin[a,d], S. Martoiu[b], G. Mazza[b], M. Noy[a], F. Petrucci[c], P. Riedler[a], A. Rivetti[b], S. Tiuraniemi[a]

[a] CERN, CH-1211 Geneva 23, Switzerland
[b] INFN Sezione di Torino, Italy
[c] INFN Sezione di Ferrara, Italy
[d] UCL, Louvain-la-Neuve, Belgium

Abstract

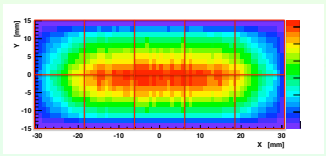
The aim of the NA62 experiment is to study the ultra rare decay of the positively charged K meson into a pion and a neutrino-antineutrino pair at the CERN SPS. The beam spectrometer has to sustain high and non-uniform beam rate (up to 1.5 MHz/mm² in the center and 0.8-1.0 GHz in total, hence the name Gigatracker) and should preserve beam divergence and limit beam hadronic interactions. The Gigatracker has to provide precise momentum, time and angular measurements on every single track of the secondary 75 GeV/c hadron beam with a timing precision of 150 ps (rms). To meet these requirements, three hybrid silicon pixel detector stations will be installed in vacuum. The readout pixel ASICs, in 130 nm CMOS technology, comprise arrays of 1800 pixels of 300×300 μm^2 and will be bump-bonded to a 200 μm thick, 60×27 mm^2 wide, p-in-n silicon sensor. An adequate strategy to compensate the discriminator time-walk must be implemented and R&D investigating two different options is ongoing. Two read-out chip prototypes have been designed in order to have an experimental comparison of the performances: one approach is based on the use of a constant-fraction discriminator followed by an on-pixel TDC, while the other one is based on the use of a Time-over-Threshold circuit followed by a TDC shared by a group of pixels. Specifications of this detector are very challenging: especially time resolution is an unusual requirement for traditional pixel detectors and none of the existing systems has such a capability. In addition the maximum calculated fluence for 100 days of data taking is comparable to the one expected in the silicon trackers in LHC experiments during 10 years of operation. The current presentation will describe the physics requirements on the Gigatracker performance and the technology choice, review the R&D project status and discuss the global architectures of both front-end ASICs.

The NA62 Experiment at the CERN SPS

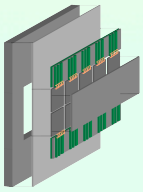


Radiation environment

- very high intensity and non-uniform hadron beam (up to 140 kHz/pixel in the center)
- calculated fluence ~2 × 10^{14} 1 MeV n equivalent/cm^2 during 100 days running time per year → comparable to those expected in inner layers of the LHC trackers



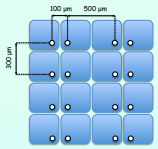
Detector Assembly



- hybrid silicon pixel detector (p-in-n)
- 300 μm × 300 μm pixel cell
- single sensor: 60 × 27 mm^2 active area
- 2 × 5 read-out chips bump bonded to the sensor
  - no dead areas and uniform material in the beam acceptance (wire bonding pads and output bus are outside the active area)
  - 1800 pixel cells per read-out chip
- total material budget < 0.5% X_0
  - 200 μm thick sensor (constrained by signal amplitude)
  - read-out wafers target thickness: < 100 μm
  - detector operated in vacuum

Bump Bonding

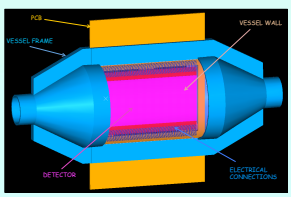
- octagonal bump bonding pads: 26 μm with 20 μm passivation opening
- pad arrangement scheme: mirrored bump pads on neighboring columns
- bonding of the prototype read-out chips (ROCs)
  - prototype ROCs will be available as single dies from MPW run
- bonding of the final assemblies that will be installed for data taking
  - final ROCs will be available as full wafers
  - thinning of final ROCs below 100 μm needed



Cooling

- sensor operating temperature < 5 °C (in vacuum) to limit the leakage current increase induced by radiation damage
- cooling options currently under study:

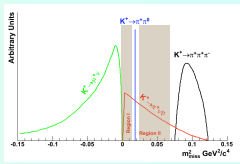
1. thin support/heatsink of very high thermal conductivity carbon fibers with high performance thermal interface material (cooling system surrounding the rectangular beam active area) and micro channel cooling in silicon substrates
2. vessel with thin cylindrical kapton walls (<100 μm) where nitrogen is circulated → quite uniform temperature distribution across sensor area



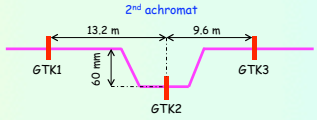
The measurement

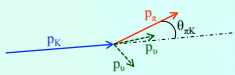
- $K^+ \to \pi^+ \upsilon \bar{\upsilon}$: process predicted with high accuracy in the Standard Model
- BR($K^+ \to \pi^+ \upsilon \bar{\upsilon}$) = (8.5 ± 0.7) × 10^{-11} in the SM
- constrain the CKM triangle only from the Kaon sector
- very sensitive to physics beyond the Standard Model
- collect O(100) $K^+ \to \pi^+ \upsilon \bar{\upsilon}$ events in about two years of data taking
- main background from $K_{\mu 2}$ and $K^+ \to \pi^+\pi^0$
- 3 handles on background reduction:
  - missing mass cuts
  - photon vetoes
  - particle identification
- redundant measurements to control the background

$$m^2_{miss} \equiv m^2_K\left(1-\frac{|p_\pi|}{|p_K|}\right)+m^2_\pi\left(1-\frac{|p_K|}{|p_\pi|}\right)-|p_K||p_\pi|\theta^2_{\pi K}$$



The beam spectrometer: GigaTracKer (GTK)





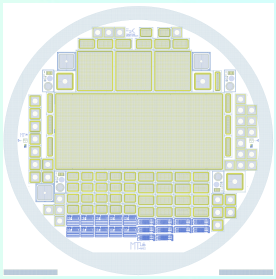
- preserve beam divergence for precise momentum and angular downstream measurements and limit beam hadronic interactions
- sustain high and non-uniform rate (up to 1.5 MHz/mm² in the center and 0.8-1.0 GHz in total)
- provide precise momentum, time and angular measurements on all beam tracks

→

- $X/X_0 << 1\%$
- pixel size 300 μm × 300 μm
- $\sigma(p_K)/p_K \sim 0.4\%$
- $\sigma(\theta_{\pi K}) \sim 17$ μrad
- $\sigma(t) \sim 150$ ps on single track

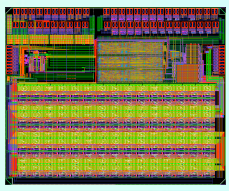
Sensor Wafer

- p-in-n sensor processing at FBK-irst (Italy)
- 4" high resistivity FZ silicon wafers
- 200 μm thickness
- bow < 30 μm to comply with flip chip bonding requirements
- depletion voltage < 30 V
- operation voltage 300 – 500 V
- multi-guard ring structure
- wafer contains:
  - one full-size sensor
  - a few single chip-size sensors
  - structures to match read-out chip prototypes
  - "dummy" read-out chips to test bump bonding process for single dies
  - diodes and other test structures
- irradiation of diodes with fast neutrons and protons
- annealing measurements (I-V and C-V) following run scenario

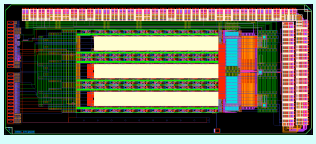


Pixel read-out ASICs

- highly complex functionality to provide unprecedented time resolution (~200 ps for single hit)
- 0.13 μm CMOS technology → long term availability, high density, high speed, low power
- huge data flow: data rate per read-out chip ~4 Gbit/s
- power dissipation ~2W/cm^2 (estimated)
- Two read-out architectures under development
  - test prototypes in 0.13 μm CMOS technology in production



- "on-pixel TDC" option
- time walk compensation: constant-fraction discriminator (CFD)
- time measurement: on-pixel TAC based TDC
- reference clock: 160 MHz
- four event buffers for data de-randomization
- SEU protected control logic (Hamming encoding)
- each pixel operates independently
- clock signal distributed to each pixel
- complex pixel circuitry
- per-pixel calibration required



- "end-of column TDC" option
- time walk compensation: Time-over-Threshold correction (TOT)
- time measurement: DLL based TDC at the end of column (EoC)
- reference clock: 320 MHz
- low power pixel circuitry
- pre-emphasis for signal transmission
- DLL based TDC plus column registers implemented
- hit arbitration circuitry at the EoC